IN THE ABSTRACT:

Please replace the specification with the attached replacement abstract on the next page.

ABSTRACT

The disclosure concerns a semiconductor memory device including a plurality of transistors. Each of the transistors has a first data state having a first threshold voltage and a second data state having a second threshold voltage. A sense amplifier is provided for a plurality of bit lines connected to drain diffusion regions of the transistors, one of the bit lines being connected to the sense amplifier. The first data state is a state in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by this impact ionization are held in the semiconductor layer. The second data state is a state in which a forward bias is applied between the semiconductor layer and the drain diffusion region to extract the excessive majority carriers from within the semiconductor layer to the drain diffusion region.